ABSTRACT

An output clock is provided by a logic module and at least one flip-flop based on a reference clock. Each flip-flop receives the reference clock at a corresponding clock end and changes a signal level outputted at a corresponding output port according to rising or falling edges within each period of the reference clock. The logic module performs a logic operation among signals at each output port of the flip-flops to generate the output clock synchronized with the reference clock. Thereafter the output clock can be outputted through the data path provided by the logic module, and additional logical operations can be performed between the output clock and other signals.